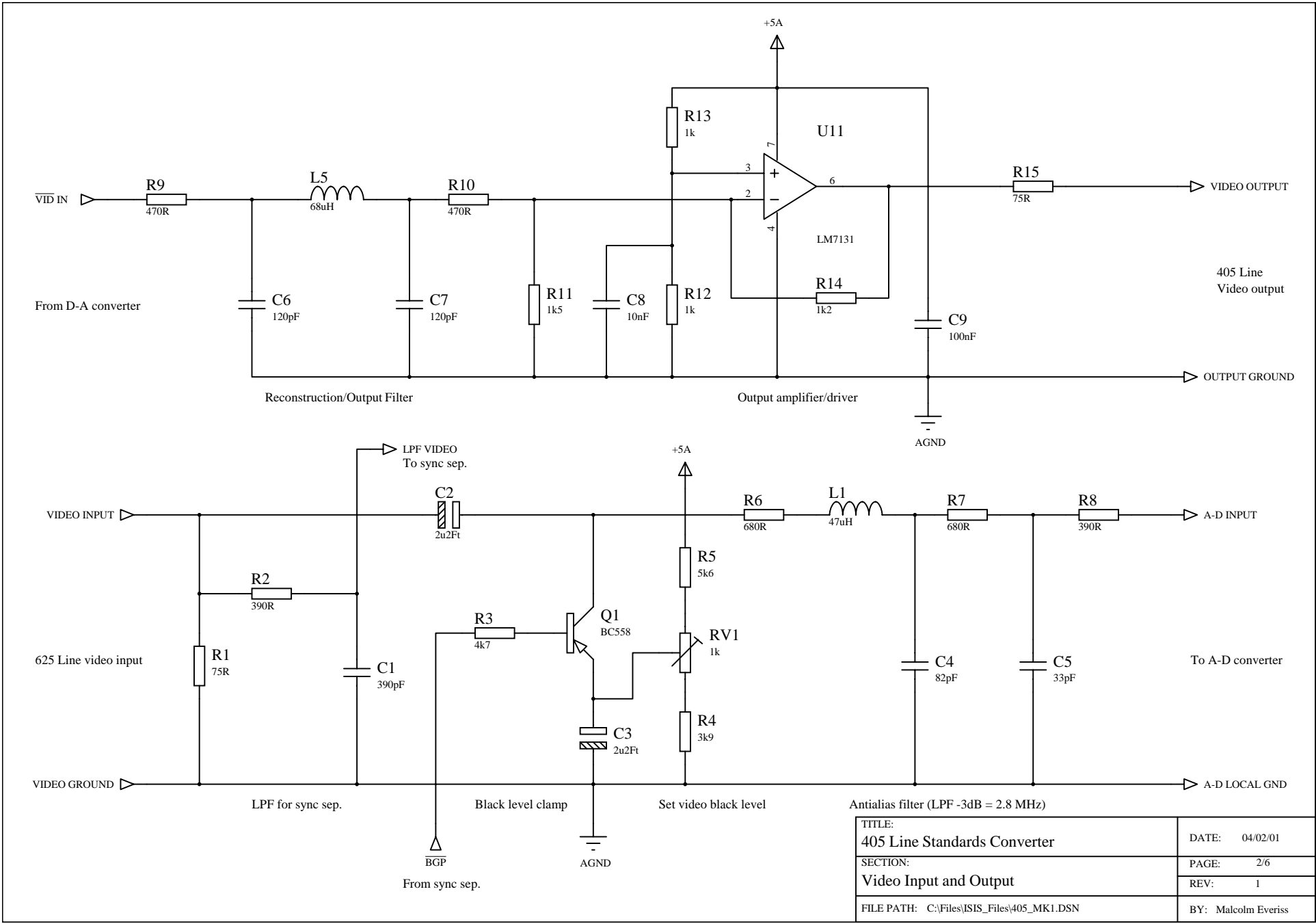
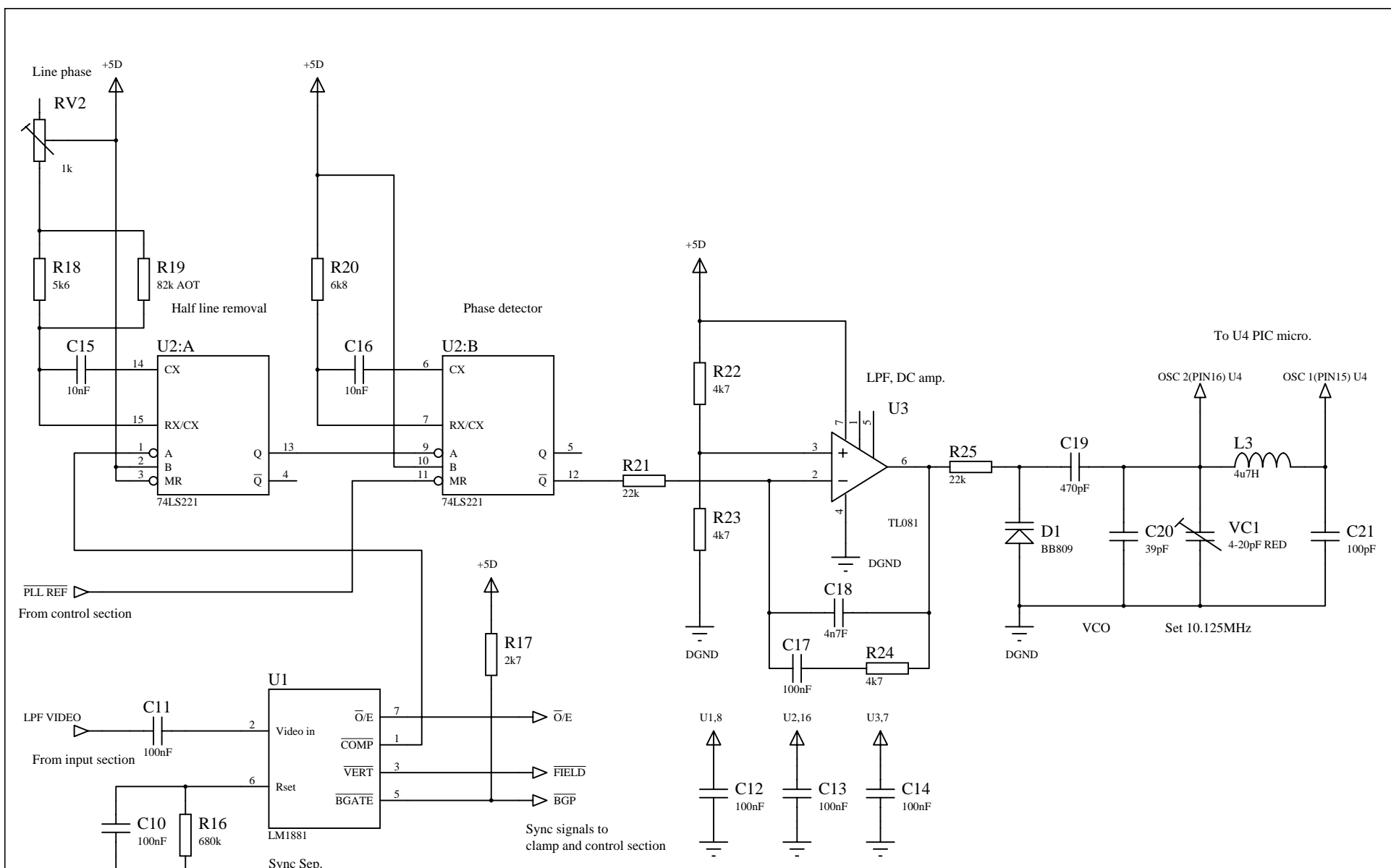


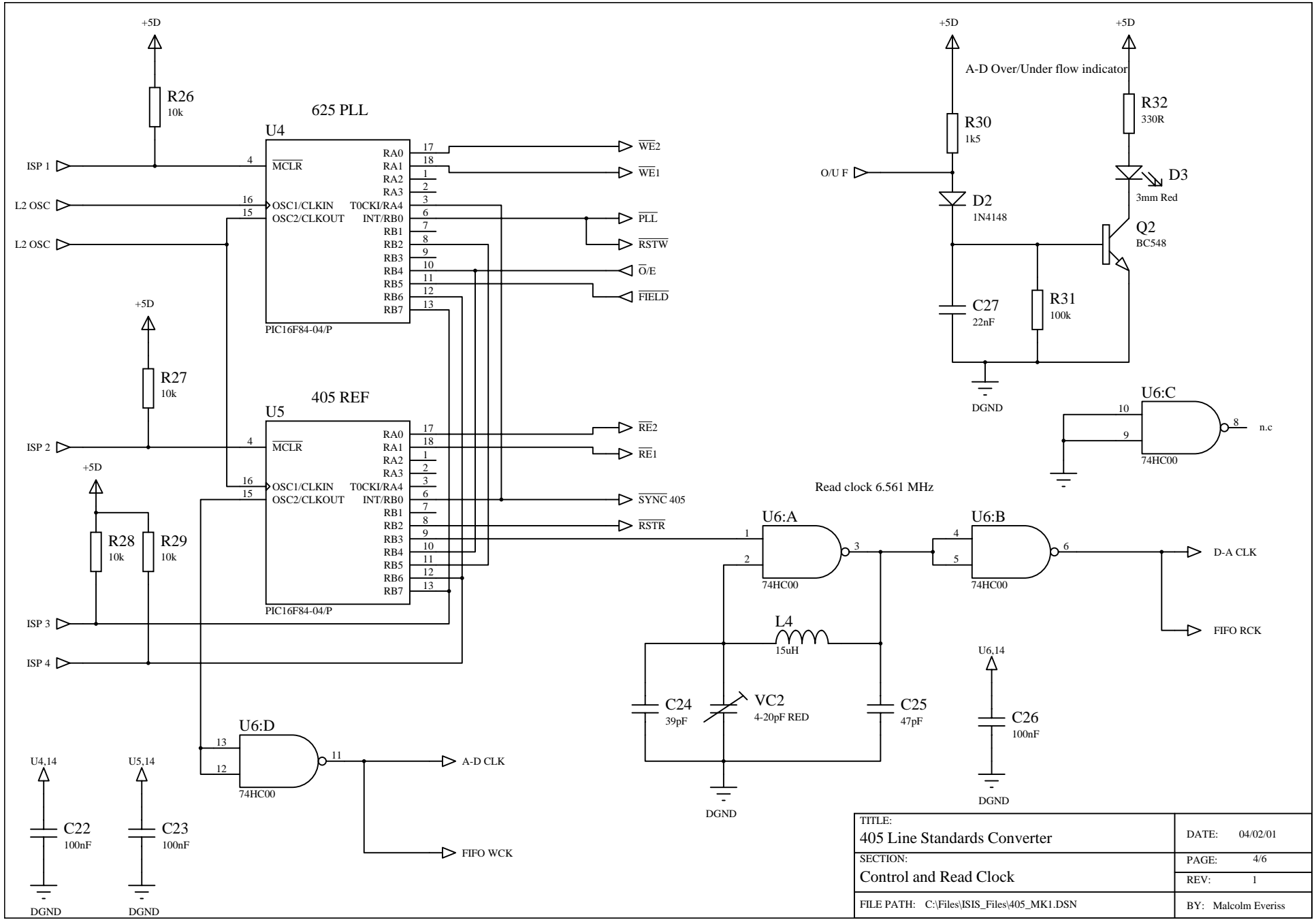
TITLE: 405 Line Standards Converter	DATE: 04/02/01
SECTION: Block Diagram	PAGE: 1/6
FILE PATH: C:\Files\ISIS_Files\405_MK1.DSN	REV: 1
	BY: Malcolm Everiss



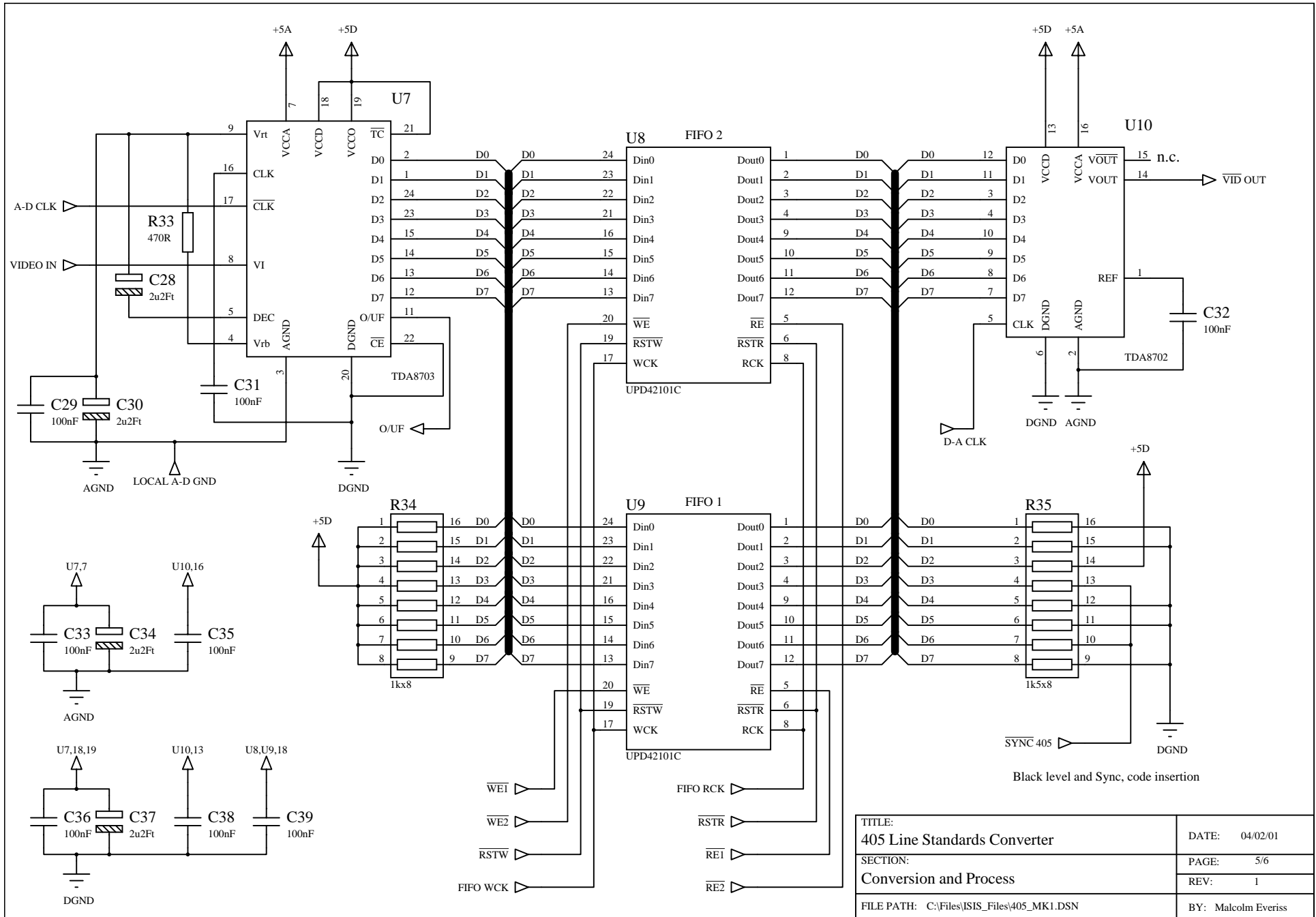
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SECTION: Video Input and Output	PAGE: 2/6
FILE PATH: C:\Files\ISIS_Files\405_MK1.DSN	REV: 1
	BY: Malcolm Everiss



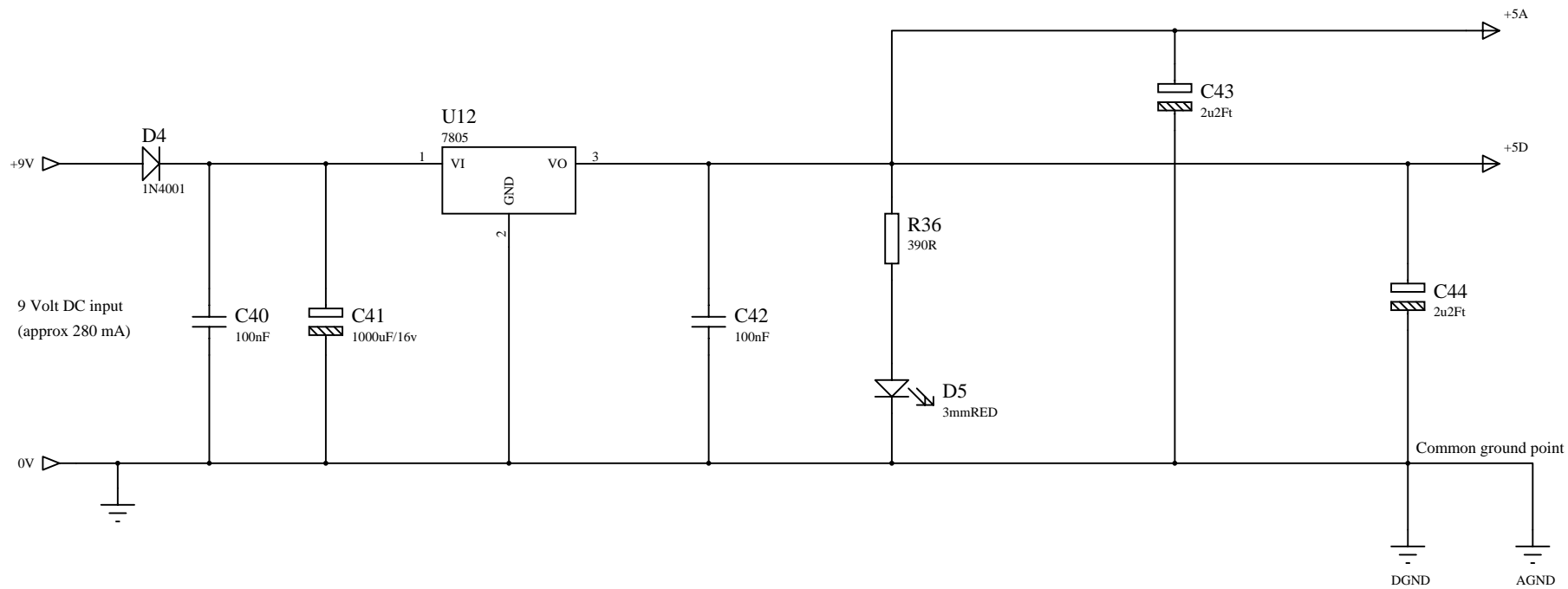
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SECTION: Sync Sep and 10.125MHz PLL	PAGE: 3/6
FILE PATH: C:\Files\ISIS_Files\405_MK1.DSN	REV: 1
	BY: Malcolm Everiss



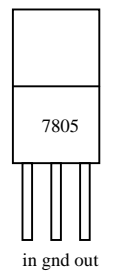
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SECTION: Control and Read Clock	PAGE: 4/6
FILE PATH: C:\Files\ISIS_Files\405_MK1.DSN	REV: 1
	BY: Malcolm Everiss



TITLE: 405 Line Standards Converter	DATE: 04/02/01
SECTION: Conversion and Process	PAGE: 5/6
FILE PATH: C:\Files\ISIS_Files\405_MK1.DSN	REV: 1
	BY: Malcolm Everiss



9 Volt DC input
(approx 280 mA)



TITLE: 405 Line Standards Converter	DATE: 04/02/01
SECTION: Power Supply	PAGE: 6/6
FILE PATH: C:\Files\ISIS_Files\405_MK1.DSN	REV: 1
	BY: Malcolm Everiss